A Monolithic Single-Chip *X*-Band Four-Bit Phase Shifter

YALCIN AYASLI, MEMBER, IEEE, ARYEH PLATZKER, MEMBER IEEE, JAMES VORHAUS, AND LEONARD D. REYNOLDS, JR.

Abstract — *X*-band GaAs monolithic passive phase shifter with 22.5°, 45°, 90°, and 180° phase bits are developed using FET switches. By cascading all four bits, a four-bit digital phase shifter with 5.1 ± 0.6-dB insertion loss is realized on a single $6.4 \times 7.9 \times 0.1$-mm chip.

I. Introduction

THE USE OF FET's as microwave switches has been reported earlier [1]–[4]. In this paper we will describe the use of such FET switches in two different types of GaAs monolithic passive phase shifter bits. We will also describe the fabrication and performance of a single-chip MMIC *X*-band four-bit passive phase shifter formed by cascading these switch FET circuits.

The basic switch element, a single-pole single-throw circuit in shunt mode of operation is shown in Fig. 1(a). The FET switch is a three-terminal device with the gate voltage V_G controlling the switch states. In a typical switch mode, the high impedance state (switch closed) corresponds to a negative gate bias larger in magnitude than the pinchoff voltage ($|V_g| > |V_p|$), and the low-impedance state (switch open) corresponds to zero gate bias. These two linear operation regions of the FET are shown schematically in Fig. 1(b). Note that in either state virtually no dc bias power is required. Therefore, the switches can practically be classified as passive as far as the overall power consumption is concerned.

Although the FET itself is a three-terminal device, the switch is bidirectional. The equivalent circuit for the two states of the switch can be represented as shown in Fig. 2, for a typical 1000-μm switch FET. These values are dependent on the channel geometry, channel doping, and pinchoff voltage of the device. The important point to note about this equivalent circuit is the following. Gate-drain and gate-source capacitances are equal because both source and drain terminals are at ground potential. As a consequence of this, the drain terminal is not isolated from the gate terminal: the RF impedance of the gate bias circuit very much affects the equivalent drain-source impedance. In the present design, the gate bias circuit is configured as a two-section low-pass filter providing an effective RF open to the FET at the gate terminal. With this approach, the

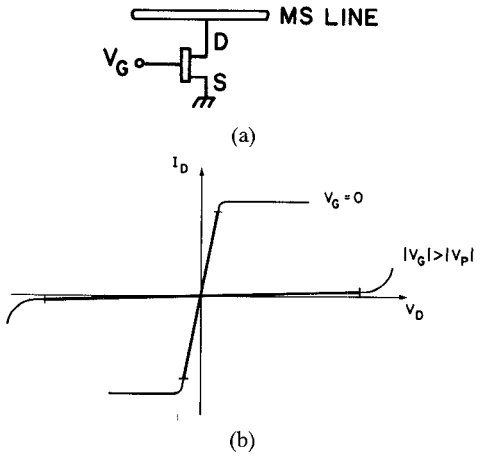

Fig. 1. (a) Basic GaAs switch in shunt mode of operation. (b) Switch FET linear operating regions.

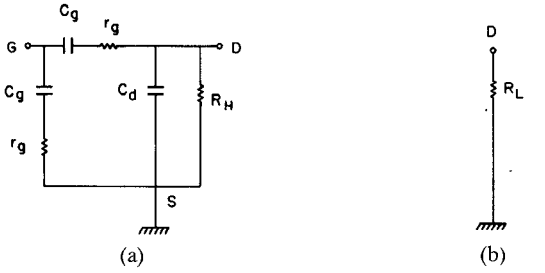

Fig. 2. Equivalent circuit used in the designs for a switch FET. (a) High resistance state; (b) low resistance state. $R_L = 3\ \Omega$, $R_H = 3\ \text{k}\Omega$, $C_d = 0.2$ pF, $r_g = 1.6\ \Omega$, $C_g = 0.2$ pF.

equivalent drain–source capacitance can simply be approximated as $C_d + C_g/2$.

Note that, unlike the p-i-n diode, the total capacitor shunting of high impedance R_H represents a reactance of the order of 50 Ω at *X*-band frequencies. Therefore, to realize the switching action, thus capacitance must be either resonated or its effect must be included in the design of the impedance-matching sections. This represents an important design consideration for FET switches as it directly relates to the frequency bandwidth of operation.

II. Four-Bit Phase-Shifter Circuit

The schematic circuit diagram of the four-bit phase shifter is shown in Fig. 3. The 22.5° and 45° bits are designed to provide constant phase shifts over the frequency bandwidth using the loaded-line technique. Each loading

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Y. Ayasli, J. Vorhaus, and L. D. Reynolds are with the Raytheon Company Research Division, Lexington, Ma 02173.

A. Platzker is with the Raytheon Company, Missile Systems Division, Bedford, MA 01730.

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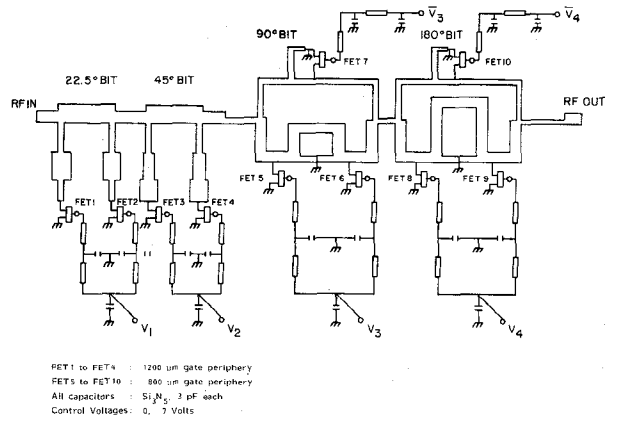

Fig. 3. The schematic circuit diagram of the four-bit phase shifter.

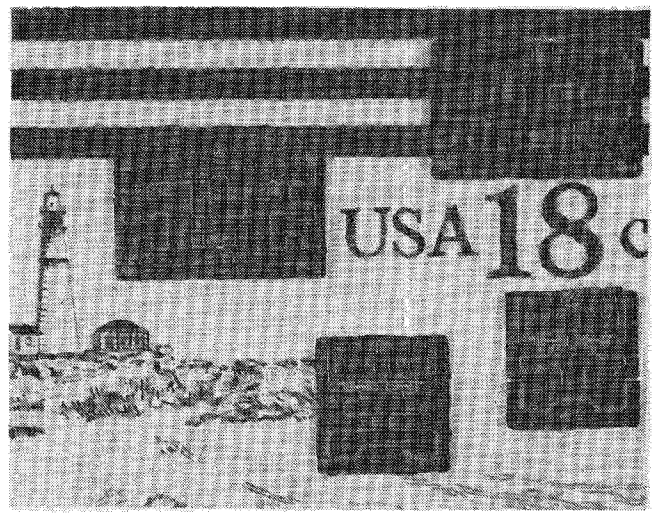

Fig. 4. Picture of individual phase bit circuits.

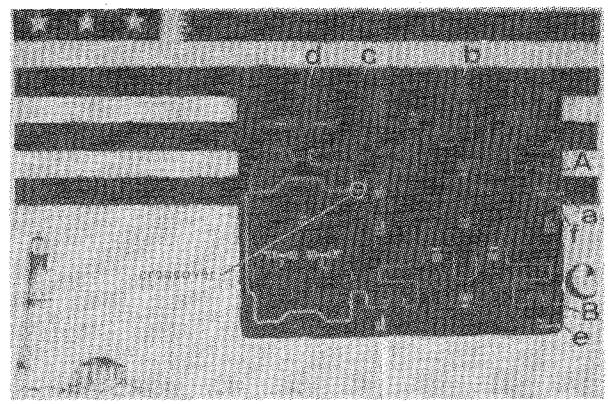

Fig. 5. Four-bit passive phase shifter chip. A = RF input/output, B = RF output/input, $a = 180°$ bit reference arm control signal, $b = 180°$ bit phase delay arm control signal, $c = 22.5°$ bit control signal, $d = 45°$ bit control signal, $e = 90°$ bit reference arm control signal, $f = 90°$ bit phase delay arm control signal.

stub is composed of a suitably designed three-section transforming and matching network which is terminated by a 1200-μm switch FET. The principle of operation of our circuits and of the ones using p-i-n diodes is the same. Both utilize the fact that the phase of a signal passing through a loaded transmission line is a function of that load. A phase shift is obtained when the load is altered between two states. If the main line is symmetrically loaded, it is possible to obtain, over appreciable bandwidths, phase shifts at approximately constant insertion losses and low input and output VSWR. In order to do so, the loads seen by the main RF line at the two phase states must assume two distinct values. In general, the impedances of the switching elements, whether they are p-i-n diodes or MESFET's, do not present the proper impedances to the main line and thus require transformation. The transformation is bilinear and its physical realization constitutes the design of the circuits.

The 90° and 180° bits are designed using the switched-line technique. Switching between lines of different electrical lengths is accomplished by two single-pole double-throw (SPDT) switches similar in principle of operation to the X-band bidirectional switch reported earlier [4]. Note, however, that instead of the conventional four switching elements, only three 800-μm switch FET's are used in these circuits. Equal insertion loss between two phase states is maintained by designing the short and long arms of the phase shifter at different impedance levels.

The insertion loss in the long arm of the phase shifter has contributions from three sources. These are the microstrip line losses, the OFF-state losses of the two FET's in the long arm, and the ON-state loss of the FET in the short arm. The insertion loss of the short arm has contributions from the microstrip line losses, the OFF-state loss of the FET in the short arm, and the ON-stage losses of the two FET's in the long arm. If the line impedances are chosen equal in both arms, then the insertion loss of the long arm is always greater than the insertion loss of the short arm. By increasing the impedance level of the short arm, however, its insertion loss can be increased, while the contribution of the ON-state loss of the FET in the short arm to the long arm insertion loss is decreased. Thus, it is possible to use only three switching FET's for the switched line phase shifter and still equalize the insertion losses of the two phase states.

TABLE I
FOUR-BIT PASSIVE PHASE SHIFTER STATISTICS

Chip Size:	6.4 x 7.9 x 0.1 mm
Number of Ports (all have integral beam leads):	
rf:	2
Control Signal:	6
Number of FETs:	10
Total Gate Periphery (Gate Length = 1 µm):	9.6 mm
Number of Capacitors (3 pF each):	16
Number of Air Bridges:	77
Number of Via Holes:	26
Total Transmission Line Length:	13.9 cm (5.5 in.)

In the present design, the long arms of both 90° and 180° phase bits are 58-Ω MS lines, whereas the 90°-bit short arm is a 74-Ω line, and the 180°-bit short arm is an 86-Ω line. The increase from 74 Ω to 86 Ω reflects the need for additional loss compensation for the 180° bit. To minimize the total gate periphery used, the 90° and 180°

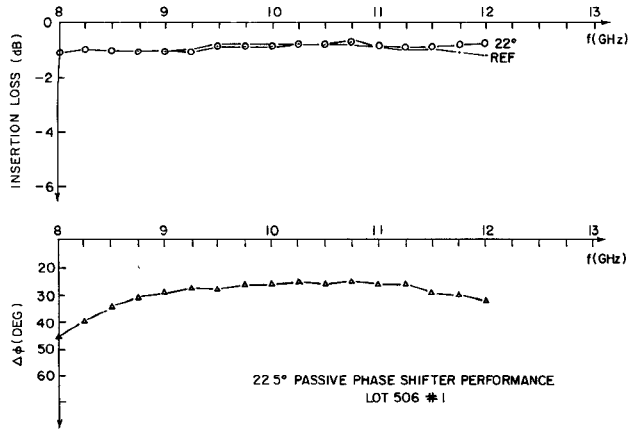

Fig. 6. 22.5° passive phase shifter performance (not corrected for jig losses).

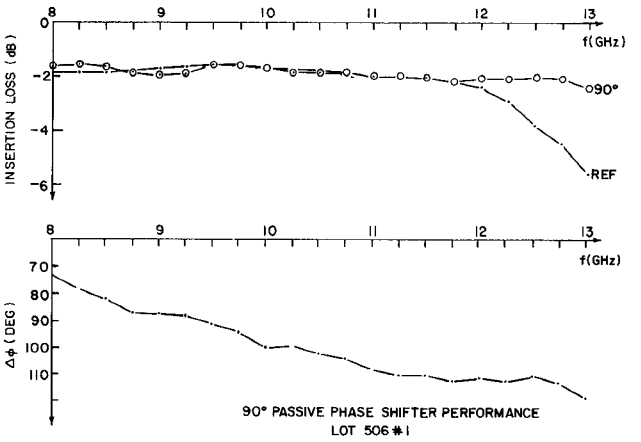

Fig. 8. 90° passive phase shifter performance (not corrected for jig losses).

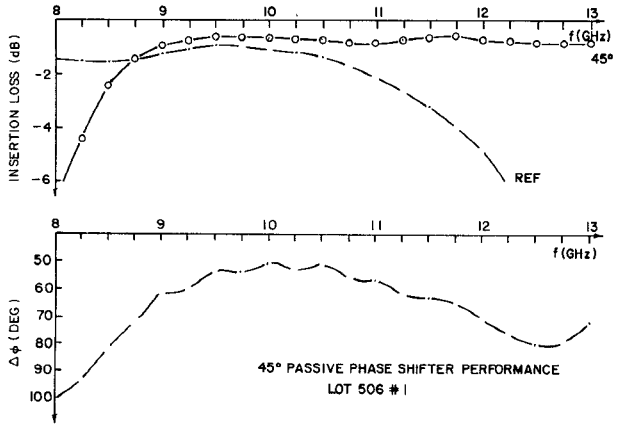

Fig. 7. 45° passive phase shifter performance (not corrected for jig losses).

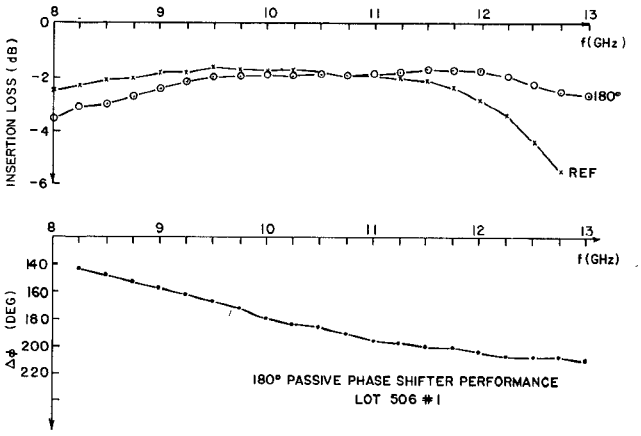

Fig. 9. 180° passive phase shifter performance (not corrected for jig losses).

phase bits are designed at the 65-Ω impedance level. The transformation back to 50-Ω is achieved by one-section impedance transformation.

For all bits, the switching is performed only through the gate control voltages and no other bias is required for the operation of the phase shifter. Thus, RF microstrip lines do not carry any dc voltage (in fact they are dc grounded) and therefore there is no need for dc blocking capacitors between individual phase bit circuits.

The realization of the individual phase shifter bits are shown in Fig. 4. The chip size is $3.15 \times 4.95 \times 0.1$ mm for the larger bits and $3.15 \times 3.15 \times 0.1$ mm for the smaller bits.

The four bits are cascaded to form a complete phase shifter on a single $6.4 \times 7.9 \times 0.1$-mm GaAs chip (Fig. 5). Starting in the upper right with the 180° bit, the microwave signal travels counterclockwise through the 45° (upper left), 22.5° (lower left), and 90° (lower right) bits, exiting on the right edge of the chip. The circuit is passive and reciprocal so that the signal can equally well traverse this path in the opposite direction.

As identified in Fig. 5, there are two control lines for each of the larger bits and one control line for each of the smaller bits. Also seen in the figure is the one crossover necessary in the circuit where the RF line between the 180° and 45° bits crosses the line connecting the control port of the 22.5° bit with the chip edge. All the necessary gate bias circuitry including RF bypass capacitors is provided monolithically on the GaAs chip, with integral beam leads for RF and control lines at the edge of the chip. The FET switches in each phase bit have a total gate periphery of 2.4 mm. The four-bit passive phase shifter chip statistics are summarized in Table I.

III. Circuit Fabrication

Circuits are processed on vapor phase epitaxy layers grown by the $AsCl_3$ system on semi-insulating GaAs substrates. The three layer structures consist of a high-doped contact layer ($n > 2 \times 10^{18} cm^{-3}$, $t = 0.2$ μm), an active layer of moderate doping ($n = 9 \times 10^{16} cm^{-3}$, $t = 0.4$ μm), and an undoped buffer region ($n < 5 \times 10^{13} cm^{-3}$, $t = 2.0$ μm). Device isolation is achieved with a combination of a shallow mesa etch and a damaging $^{16}O^{+}$ implant.

Ohmic contacts are formed by alloying the standard Ni/AuGe metallization into the surface. The ohmic metal also forms the bottom plates of the thin-film capacitors. The gates, which are recessed, consist of a Ti/Pt/Au (1000/1000/3000 Å) metallization and are nominally 1 μm long.

The capacitor dielectric is a plasma-assisted CVD silicon nitride layer with a nominal thickness of 5000 Å and a relative dielectric constant of 6.8. The final frontside processing steps define the transmission line structures, capacitor top plates and air-bridge interconnects. All of these are fabricated out of plated gold about 3 to 4 μm thick. The air-bridges are used to connect from the GaAs surface to the top plates of the MIM capacitors without having to cross the dielectric step and risk shorting of the structure.

After plating, the wafer is lapped to its final thickness of 100 μm by first mounting it upside down on an alumina substrate. Via-holes are etched through the wafer to ground points on the frontside. The via-holes are aligned by looking through the slice with infrared optics to see the frontside pattern. Finally, a chip dicing grid is defined in the back by alignment to the via-hole pattern and the region between the grid lines (the chip back) is plated to a thickness of 12 to 15 μm with gold. The grid lines are etched through to the frontside, the wafer dismounted, and the chips allowed to simply fall apart.

IV. The Experimental Performance

The insertion loss and relative phase shift for each of the four bits are presented in Figs. 6 to 9. None of the insertion-loss data is corrected for the approximately 0.5-dB test fixture loss. The differential phase shift follows the linear phase versus frequency behavior for the switched line 90° and 180° phase bits and the constant phase versus frequency behavior for the 22.5° and 45° loaded-line phase bits. The phase error at around 10 GHz is less than 10° for any bit.

The four individual phase shifter bits are cascaded to form a complete phase shifter. The text fixture with the circuits is shown in Fig. 10. The overall insertion loss for each of the sixteen phase states is shown in Fig. 11. There is about 0.5 dB of test fixture loss which has not been subtracted from this data. The cascaded phase shifter thus has slightly less than 5 dB of total insertion loss with a variation over all states of less than ± 0.3 dB across the design band. Fig. 12 shows the relative phase shift of each of the phase shifter states.

Encouraged by the performance of the cascaded circuit, we have fabricated the first single-chip four-bit passive phase shifter circuit, described earlier.

This single-chip four-bit phase shifter is characterized in the measurement jig shown in Fig. 13.

Fig. 14 shows the insertion loss (not corrected for approximately 1 dB of jig losses) for all 16 states. At 9.5 GHz, the insertion loss is 5.1 ± 0.6 dB. Fig. 15 shows the differential phase shift in the 8.5- to 10.5-GHz frequency band. The circuit is matched to 50-Ω input and output system with better than 10-dB return losses for all 16 states over the 2.5-GHz frequency band.

The phase linearity of the reference state is also measured. Deviation of phase around a defined zero is less than $\pm 10°$ for larger than 3-GHz frequency band.

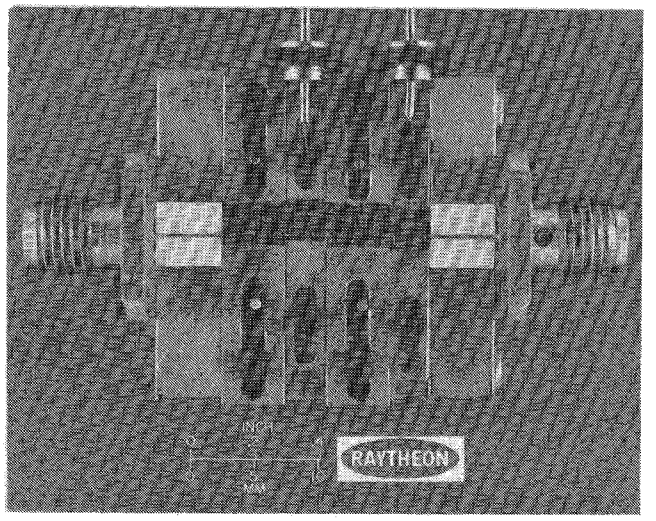

Fig. 10. Cascaded passive phase shift bit chips in test fixture.

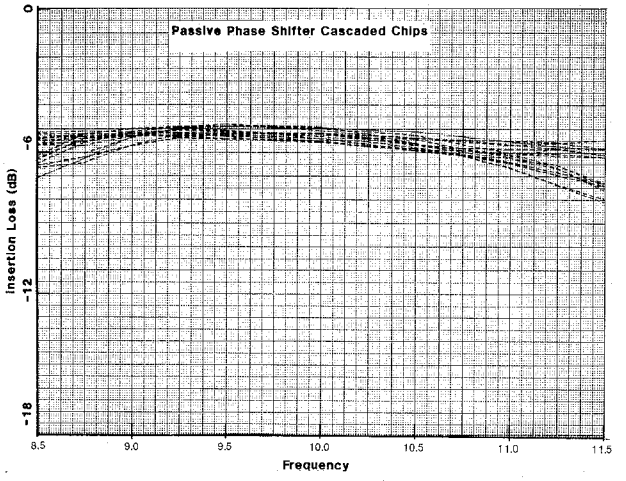

Fig. 11. Passive phase shifter cascaded chips insertion loss performance (not corrected for jig losses).

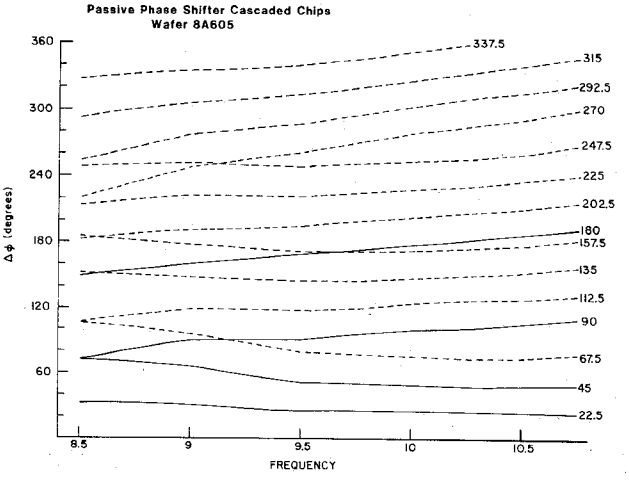

Fig. 12. Passive phase shifter cascaded chips differential phase performance.

Total RMS phase error of the four-bit phase shifter and the predicted performance of a typical airborne phased-array antenna system utilizing this monolithic phase shifter

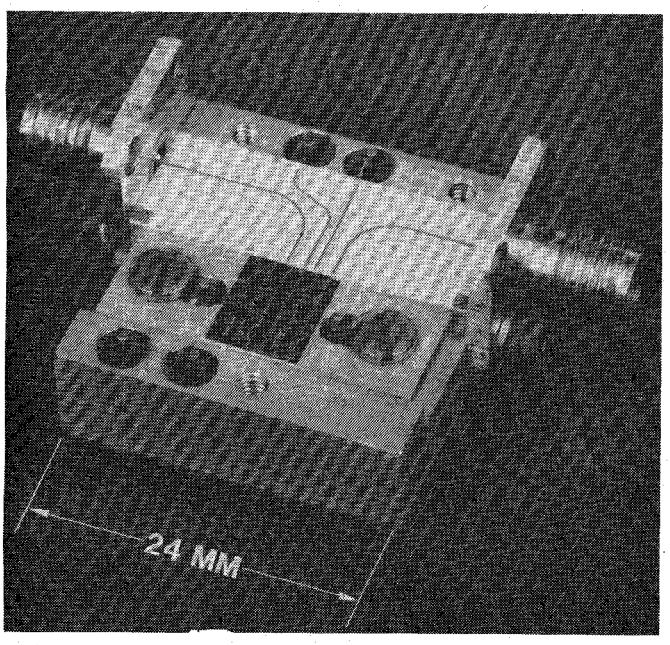

Fig. 13. Measurement jig for the single-chip four-bit phase shifter.

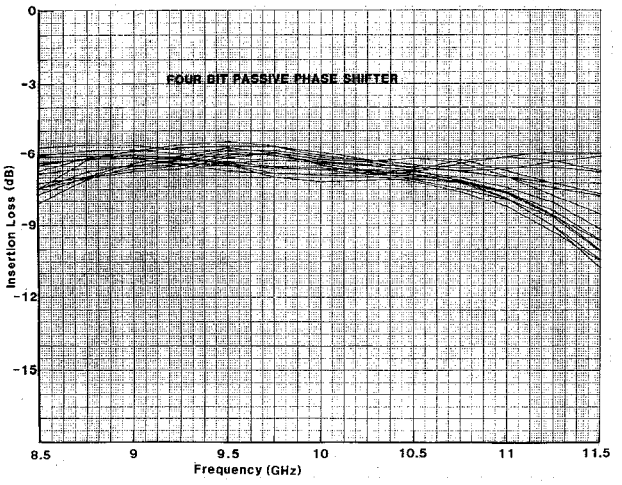

Fig. 14. Insertion loss for all 16 states of a four-bit passive phase shifter (no correction for jig losses has been made).

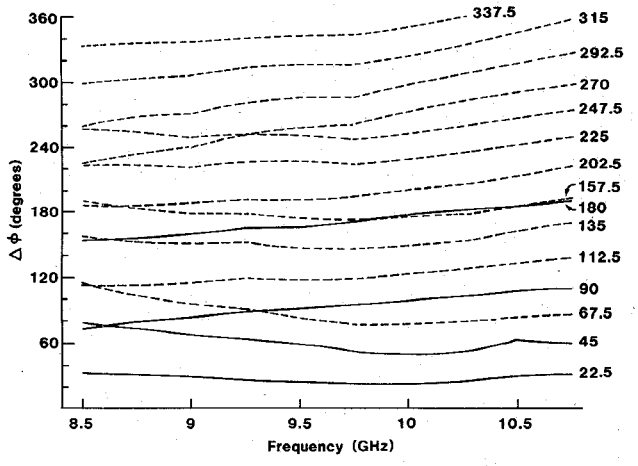

Fig. 15. Phase shift versus frequency for all 15 nonzero states of a four-bit passive phase shifter.

TABLE II
ARRAY RANDOM ERROR EFFECTS BASED ON FOUR-BIT PASSIVE MONOLITHIC PHASE SHIFTER DATA (100 ARRAY ELEMENTS ARE ASSUMED)

Frequency (GHz)	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0
Total rms Phase Error (σ_T)	39.4°	25.4°	17.3°	11.4°	8.7°	11.1°	14.7°	17.6°	13.1°
Gain Reduction (dB) (G/G_0)	-1.7	-0.8	-0.4	-0.2	-0.1	-0.2	-0.3	-0.4	-0.5
rms Sidelobe Level (dB) (SLL)	-23.3	-27.1	-30.4	-34.0	-36.4	-34.3	-31.8	-33.9	-29.5
Beam Pointing Error (%) $\Delta\theta/\theta$ 3 dB	6.9	4.4	3.0	2.0	1.5	1.9	2.6	3.1	3.3

is summarized in Table II. The results indicate that the predicted performance is satisfactory for typical phase array requirements.

V. CONCLUSION

An *X*-band GaAs monolithic phase shifter with 22.5°, 45°, 90°, and 180° phase bits has been made using GaAs switch FET's. By cascading all four bits on the same chip, a digital passive phase shifter with 5.1 ± 0.6-dB insertion loss and 16 distinct phase states between 0° and 360° is realized. The performance of the phase shifter is satisfactory for typical phased array applications. Their small size, negligible dc power requirement, and subnanosecond switching times make these monolithic phase shifters prime candidates for future frequency agile airborne phase array systems.

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Yalcin Ayasli (M'79) received the B.S. degree from Middle East Technical University in Ankara, Turkey, in 1968. His graduate study was at Massachusetts Institute of Technology, Cambridge, MA, where he received the M.S. degree in 1970 and the Sc.D. in 1973, both in electrical engineering. His doctoral thesis research on "Magnetic Semiconductor Interactions" was performed with the microwave and quantum magnetics group at M.I.T.

From 1973–1979 he was a member of the faculty of Engineering at Middle East Technical University. His teaching responsibilities included undergraduate and graduate courses on electromagnetic theory, microwave theory, and the electrodynamics of waves, media, and interactions. In September 1979 Dr. Ayasli joined the semiconductor laboratory of the Raytheon Research Division, where he has been actively engaged in theoretical and experimental studies of micro-

wave monolithic integrated circuit techniques involving field-effect transistors and related devices.

Dr. Ayasli is the author of a number of technical papers.

✤

Aryeh Platzker (M'79) was born in 1939 in Haifa, Israel, and graduated from the Technion, Israel Institute of Technology in 1963. From 1964 to 1970 he has been pursuing graduate studies at the Massachusetts Institute of Technology where he received the S.M. and Ph.D. degrees from the Electrical Engineering Department in 1967 and 1970, respectively. In the years 1970 to 1972 he was a Postdoctoral Fellow at the Center for Material Science and Engineering at M.I.T.

He was employed at Chu Associates prior to joining the Raytheon Corporation in 1978. His areas of research included electromagnetic and ultrasonic wave propagation and interaction in magnetic materials. Since 1978 he has been engaged in the area of monolithic microwave semiconductor circuits. His contributions include the development of CAD methods and programs for both design and characterization as well as the design, characterization, and processing of novel monolithic circuits.

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James Vorhaus received the B.S. degree in engineering physics from Lehigh University in 1972 and the M.S. and Ph.D. degrees in physics from the University of Illinois at Urbana-Champaign in 1974 and 1976, respectively.

From 1973 to 1976 Dr. Vorhaus was a Research Assistant in a low-temperature physics laboratory at the University of Illinois. His work involved state-of-the-art measurements of the specific heat and thermal conductivity of various materials at very low temperatures and resulted in a better understanding of the nature of the electron-phonon and phonondislocation interactions in metallic systems. In 1976 Dr. Vorhaus joined the Raytheon Research Division as a member of the Semiconductor Laboratory. His responsibilities have included developing and improving processing technology, ion implantation technology, and material and device evaluation techniques for low-noise single-gate, multicell high power FET's and dual-gate FET's for both small signal, and high power applications. Presently, he is Manager of a program for development of the designs of and fabrication processes for GaAs monolithic microwave integrated circuits primarily for phased-array systems.

Dr. Vorhaus is a member of APS, Phi Beta Kappa, and Tau Beta Pi.

✤

Leonard D. Reynolds, Jr., received the B.S. degree (1975, with honors) and the M.S. degree (1978, with honors) in electrical and computer engineering from Clemson University. His undergraduate course concentration was in solid-state circuits and his graduate concentration was in communication theory.

In 1978 Mr. Reynolds joined Raytheon Company, Special Microwave Devices Operation, to assist in FET evaluation, modelling, and design. In 1980 he transferred to Raytheon's Research Division, where he is engaged in evaluation and modelling of monolithic microwave integrated circuit components.

X-Band Burnout Characteristics of GaAs MESFET's

JAMES J. WHALEN, SENIOR MEMBER, IEEE, ROBERT T. KEMERLEY, MEMBER, IEEE, AND ELISEE RASTEFANO, MEMBER, IEEE

Abstract — *X*-band μs pulse, ms pulse, and CW-burnout data have been measured for two commercially available 1-μm gate GaAs MESFET's. Values of incident pulse power required to cause burnout indicate a threshold level for pulse durations 0.2 μs or longer and for CW. The incident power threshold level for burnout is in the range 3 to 6 W for the MESFET type with a Ti/Pt/Au gate metallization and in the range 1.5 to 3 W for the MESFET type with an Al gate metallization. Many MESFET's were observed to fail during a single pulse.

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J. J. Whalen and E. Rastefano are with the Department of Electrical Engineering, State University of New York at Buffalo, Amherst, NY 14226.

R. T. Kemerley is with the Avionics Laboratory, Wright–Patterson AFB, OH 45433.

I. INTRODUCTION

LOW-NOISE gallium-arsenide (GaAs) metal-semiconductor field-effect transistors (MESFET's) have been developed for use as RF amplifier stages in microwave receivers. One important application for these RF amplifier stages will be in transmit–receive radar systems which share a common antenna. Transmit–receive radar systems usually have protection devices to limit the micro-

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